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Attorney's Docket No.: 42P15685

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Is/Re Patent Application of:

Scott A. Hareland et al.

Application No.: 10/607,769

Filed: June 27, 2002

For: NONPLANAR SEMICONDUCTOR
DEVICE WITH PARTIALLY OR FULLY
WRAPPED AROUND GATE ELECTRODE
AND METHODS OF FABRICATION

Examiner: Unassigned

Art Unit: Unassigned

Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

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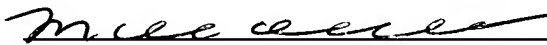
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If there are any additional charges, please charge Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: 11/11, 2004


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INFORMATION DISCLOSURE

STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet

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of

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Complete if Known

Application Number	10/607,769
Filing Date	June 27, 2003
First Named Inventor:	Scott A. Hareland
Art Unit	Unknown
Examiner Name	Unknown
Attorney Docket Number	42P15685

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Document Number		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (If known)				
		US-	6,716,684 B1	4/6/2004	Krivokapic et al.	
		US-	6,680,240 B1	1/20/2004	Maszara	
		US-	6,562,665 B1	5/13/2003	Yu	
		US-	6,525,403 B2	2/25/2003	Inaba et al.	
		US-	6,475,869 B1	11/5/2002	Yu	
		US-	5,563,077	10/8/1996	Ha	
		US-	5,346,839	9/13/1994	Sundaresan	
		US-	2002/0081794 A1	6/27/2002	Ito	
		US-	2002/0167007 A1	11/14/2002	Yamazaki et al.	
		US-	6,483,156 B1	11/29/2002	Adkisson et al.	
		US-	5,578,513	11/26/1996	Maegawa	
		US-	6,413,802 B1	7/2/2002	Hu et al.	
		US-	6,730,964 B2	5/4/2004	Horiuchi	
		US-				
		US-				

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Foreign Patent Document		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ⁶
		Country Code ³	Number ⁴ Kind Code ⁵ (if known)				
			EP 0 623 963 A1	11/9/1994	Siemens AG		
			WO 02/43151A	5/30/2002	Hitachi ULSI Sys Co Ltd		

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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. ¹Applicant's unique citation designation number (optional). ²See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. ³Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴For Japanese patent documents, the indication of the year of reign of the Emperor must precede the serial number of the patent document. ⁵Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. ⁶Applicant is to place a check mark here if English language translation is attached.

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Sheet 2 of 2

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Application Number	10/607,769
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Art Unit	Unknown
Examiner Name	Unknown
Attorney Docket Number	42P15685

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T ²
		V. Subramanian et al., "A Bulk-Si-Compatible Ultrathin-body SOI Technology for Sub-100nm MOSFETS" Proceeding of the 57th Annual Device Research Conference, pp. 28-29 (1999)	
		Hisamoto et al., "A Folded-channel MOSFET for Deepsub-tenth Micron Era", 1998 IEEE International Electron Device Meeting Technical Digest, pp 1032-1034 (1998)	
		Huang et al., "Sub 50-nm FinFET: PMOS", 1999 IEEE International Electron Device Meeting Technical Digest, pp 67-70 (1999)	
		Auth et al., "Vertical, Fully-Depleted, Surroundings Gate MOSFETS On sub-0.1um Thick Silicon Pillars", 1996 54th Annual Device Research Conference Digest, pp 108-109 (1996)	
		Hisamoto et al., "A Fully Depleted Lean-Channel Transistor (DELTA)-A Novel Vertical Ultrathin SOI MOSFET", IEEE Electron Device Letters, V. 11(1), pp36-38 (1990).	
		Jong-Tae Park et al., "Pi-Gate SOI MOSFET" IEEE Electron Device Letters, Vol. 22, No. 8, August 2001, pages 405-406	
		Hisamoto, Digh et al. "FinFET- A Self-Aligned Double-Gate MOSFET Scalable to 20 nm", IEEE Transactions on Electron Devices, Vol. 47, No. 12, December 2000, pages 2320-2325	
		International Search Report PCT/US 03/26242	
		International Search Report PCT/US 03/39727	
		International Search Report PCT/US 03/40320	